REMARKS

In the non-final Office Action, the Examiner rejected claims 1-57 under 35 U.S.C. § 102(e) as anticipated by Kovacevic et al. (U.S. Patent No. 6,674,805).

By this Amendment, Applicants amend claim 1 to improve form. Applicants respectfully traverse the Examiner's rejection under 35 U.S.C. § 102. Claims 1-57 remain pending.

In paragraphs 2-23 of the Office Action, the Examiner rejected claims 1-57 under 35 U.S.C. § 102(e) as allegedly anticipated by Kovacevic et al. Applicants respectfully traverse the rejection.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. In other words, the identical invention must be shown in as complete detail as contained in the claim. See M.P.E.P. § 2131. Kovacevic et al. does not disclose or suggest the combination of features recited in claims 1-57.

Amended independent claim 1, for example, is directed to a system for processing data received in a plurality of incoming streams of variable speeds. The system comprises a memory configured to store data associated with a plurality of incoming streams of variable speeds, an interface controller comprising a first arbitration element and configured to store the data in the memory using the first arbitration element, and a dispatch unit comprising a second arbitration element and configured to read the data from the memory using the second arbitration element.

Kovacevic et al. does not disclose or suggest the combination of features recited in amended claim 1. For example, Kovacevic et al. does not disclose or suggest a memory

configured to store data associated with a plurality of incoming streams of variable speeds. In fact, Kovacevic et al. is completely silent with regard to streams of variable speeds.

The Examiner did not specifically address this feature, but alleged Kovacevic et al. discloses each of the features recited in claim 1 and cited column 19, lines 21-29 and 47-61, of Kovacevic et al. for support (Office Action, paragraph 2). Applicants respectfully disagree.

At column 19, lines 21-29, Kovacevic et al. discloses:

> FIG. 26 includes a detailed view of buffer controller 460 of FIG. 5, video bus/memory controller 488, system bus/memory controller 468, video memory 471, and system memory 472. In the specific embodiment illustrated in FIG. 26, the buffer controller 460 includes a data path for handling video PES data to be stored in the video buffer 500 of video memory 471, and a data path for handling other PES data that is to be stored in system memory buffers 501-503 of the system memory 472.

Nowhere in this section, or elsewhere, does Kovacevic et al. disclose or suggest a memory configured to store data associated with a plurality of incoming streams of variable speeds, as required by claim 1.

At column 19, lines 47-61, Kovacevic et al. discloses:

> In accordance with the invention, the System Memory 472 has been partitioned by the system host to include one or more system circular buffers 501-503. The system buffers 501-503 are implemented as circular buffers and are filled by operation of the controller 483. The controller 483 handles the buffer "write" pointer. The "read" pointer for the buffers is managed by the software on the system host side (not shown) which retrieves data from the buffers 501-503. There can also be a "high water" mark register associated with each buffer (not shown). The purpose of a "high water" mark register is to provide an interrupt when the write pointer crosses the value in this register. However, because there is generally only one interrupt for each of the plurality of buffers, software polling can be used to determine the cause of the interrupt.

Nowhere in this section, or elsewhere, does Kovacevic et al. disclose or suggest a memory configured to store data associated with a plurality of incoming streams of variable speeds, as required by claim 1.

Because Kovacevic et al. does not disclose or suggest data associated with a plurality of incoming streams of variable speeds, Kovacevic et al. cannot disclose or suggest an interface controller comprising a first arbitration element and configured to store the data in the memory using the first arbitration element or a dispatch unit comprising a second arbitration element and configured to read the data from the memory using the second arbitration element, as also required by claim 1.

The Examiner alleged that Kovacevic et al. discloses these features and cited column 19, lines 21-29 and 47-61, of Kovacevic et al. for support (Office Action, paragraph 2). Applicants respectfully disagree.

Column 19, lines 21-29 and 47-61, of Kovacevic et al. have been reproduced above. As explained above, nowhere in these sections, or elsewhere, does Kovacevic et al. disclose or suggest data associated with a plurality of incoming streams of variable speeds. Therefore, contrary to the Examiner's allegations, Kovacevic et al. cannot disclose or suggest an interface controller comprising a first arbitration element and configured to store the data in the memory using the first arbitration element or a dispatch unit comprising a second arbitration element and configured to read the data from the memory using the second arbitration element, as required by claim 1.

For at least these reasons, Applicants submit that claim 1 is not anticipated by Kovacevic et al. Claims 2-20 depend from claim 1 and are, therefore, not anticipated by Kovacevic et al. for at least the reasons given with regard to claim 1. Claims 2-20 are also not anticipated by Kovacevic et al. for reasons of their own.

For example, claim 4 recites that the first arbitration element is configured to store a plurality of entries, where each of the entries includes a stream number that identifies one of the streams. Kovacevic et al. does not disclose or suggest the combination of features recited in claim 4.

The Examiner alleged that Kovacevic et al. discloses a first arbitration element that is configured to store a plurality of entries, where each of the entries includes a stream number that identifies one of the streams and cited column 16, lines 1-11, of Kovacevic et al. for support (Office Action, paragraph 5). Applicants respectfully disagree.

At column 16, lines 1-11, Kovacevic et al. discloses;

> In the implementation of FIG. 21, a storage location within the storage locations 751 is reserved for the STREAM ID header field of a transport stream packet. In the embodiment shown at FIG. 21, inputs of the storage location for STREAM ID are connected to the appropriate bits of the data bus and the counter controller 752, to receive stream ID data from the FRAMER DATA representation of the transport stream at the correct time. The counter controller 752 receives the VSTART signal indicating the start of a new video PES and generates enable signals to capture the stream ID, and other information, from the video PES header.

In this section, Kovacevic et al. discloses that there is a storage location for storing a STREAM ID header field. Nowhere in this section, or elsewhere, does Kovacevic et al. disclose or suggest a first arbitration element that is configured to store a plurality of entries that each includes a stream number that identifies one of the streams, where the first arbitration element is used to store data associated with the streams in the memory, as required by claim 4.

For at least these additional reasons, Applicants submit that claim 4 is not anticipated by Kovacevic et al. Claims 5-8 depend from claim 4 and are, therefore, also not anticipated by Kovacevic et al. for at least the reasons given with regard to claim 4.

In addition, claim 5 recites that the number of entries in the first arbitration element for a particular one of the streams is based on a speed of the stream. Kovacevic et al. does not disclose or suggest the combination of features recited in claim 5.

The Examiner alleged that Kovacevic et al. discloses that the number of entries in the first arbitration element for a particular one of the streams is based on a speed of the stream and cited column 31, lines 10-21, of Kovacevic et al. for support (Office Action, paragraph 6). Applicants respectfully disagree.

At column 31, lines 10-21, Kovacevic et al. discloses;

> FIGS. 39-42 illustrate a specific implementation of a method for blind synchronization to a transport stream. Blind synchronization allows the framer to acquire the transport stream, i.e. lock onto the transport stream, without any prior knowledge of the transport stream characteristics.
>
> As discussed with reference to FIGS. 8 and 9, the transport stream can include a variety of signals. At a minimum, the transport stream will include a data signal (TDATA) and a clock signal (TCLOCK). Additional signals that may exist include TSTART, TVALID, and TERROR. Based upon these signals, the transport stream has a number of characteristics, such as individual signal polarities, and data ordering.

Contrary to the Examiner's allegation, there is nothing in this section of Kovacevic et al. that discloses or remotely suggests a first arbitration element with a number of entries for a particular one of the streams based on a speed of the stream, as required by claim 5.

For at least these additional reasons, Applicants submit that claim 5 is not anticipated by Kovacevic et al.

Claim 9 recites that the first and second arbitration elements are synchronized. Kovacevic et al. does not disclose or suggest the combination of features recited in claim 9.

The Examiner alleged that Kovacevic et al. discloses first and second arbitration elements that are synchronized and cited column 8, lines 32-43, of Kovacevic et al. for support (Office Action, paragraph 10). Applicants respectfully disagree.

At column 8, lines 32-43, Kovacevic et al. discloses;

> FIG. 9 illustrates the relationship between the various control and data signals of the transport stream. Specifically, FIG. 9 illustrates a TCLOCK signal having a rising edge for qualifying each data byte of the TDATA signal. Likewise, in the illustration of FIG. 9, the TVALID signal is always asserted during the first byte indicating that the data is valid. The TSTART signal is synchronized to the first byte of the TDATA signal, which is a synchronization byte. In a specific implementation, the synchronization byte of the TDATA signal will always have the Hexadecimal value 47h. The TERROR signal is not illustrated, however it would be asserted to indicate when an error has occurred.

This section of Kovacevic et al. discloses that a TSTART signal is synchronized to a first byte of a TDATA signal. Contrary to the Examiner's allegation, there is nothing in this section of Kovacevic et al. that discloses or remotely suggests first and second arbitration elements that are synchronized, where the first arbitration element is used to store data in the memory and the second arbitration element is used to read data from the memory, as required by claim 9.

For at least these additional reasons, Applicants submit that claim 9 is not anticipated by Kovacevic et al.

Claim 10 recites features similar to features recited in claim 4, but with regard to the second arbitration element instead of the first arbitration element. Claim 10 is, therefore, not anticipated by Kovacevic et al. for at least reasons similar to reasons given with regard to claim 4. Claims 11 and 12 depend from claim 10 and are, therefore, not anticipated by Kovacevic et al. for at least the reasons given with regard to claim 10. Further, claim 11 recites features similar to

features recited in claim 5. Claim 11 is, therefore, also not anticipated by Kovacevic et al. for at least reasons similar to reasons given with regard to claim 5.

Independent claim 21 is directed to a method for processing data received in a plurality of incoming streams of variable speeds. The method comprises storing data from a plurality of variable speed streams in a memory using a first arbitration element, and reading the data from the memory using a second arbitration element.

Kovacevic et al. does not disclose or suggest the combination of features recited in claim 21. For at least reasons similar to reasons given with regard to claim 1, Kovacevic et al. does not disclose or suggest storing data from a plurality of variable speed streams in a memory using a first arbitration element, and reading the data from the memory using a second arbitration element.

For at least these reasons, Applicants submit that claim 21 is not anticipated by Kovacevic et al. Claims 22-39 depend from claim 21 and are, therefore, not anticipated by Kovacevic et al. for at least the reasons given with regard to claim 21. Claims 22-39 also recite features similar to features recited in claims 2-20. Claims 22-39 are, therefore, also not anticipated by Kovacevic et al. for at least reasons similar to reasons given with regard to claims 22-39.

Independent claim 40 is directed to a system for performing flow control on data in a plurality of incoming streams of variable speeds. The system comprises a buffer configured to temporarily store data from a plurality of streams of variable speeds in a plurality of entries, a counter configured to determine a number of entries in the buffer corresponding to each of the

streams, and a comparator configured to determine whether to initiate flow control for each of the streams based on the determined number of entries for the stream.

Kovacevic et al. does not disclose or suggest the combination of features recited in claim 40. For example, Kovacevic et al. does not disclose or suggest a buffer configured to temporarily store data from a plurality of streams of variable speeds in a plurality of entries. As explained above with regard to claim 1, Kovacevic et al. is silent with regard to steams of variable speeds. Therefore, Kovacevic et al. cannot disclose or suggest a buffer configured to temporarily store data from a plurality of streams of variable speeds in a plurality of entries, as required by claim 40.

The Examiner did not specifically address this feature of claim 40. Therefore, the Examiner did not establish a proper case of anticipation with regard to claim 40.

When rejecting claim 16, however, the Examiner alleged that Kovacevic et al. discloses a buffer configured to temporarily store data from the interface controller in a plurality of entries and cited column 15, lines 45-62, of Kovacevic et al. for support (Office Action, paragraph 17). Applicants respectfully submit that nowhere in this section, or any other section, does Kovacevic et al. disclose or suggest a buffer configured to temporarily store data from a plurality of streams of variable speeds in a plurality of entries, as recited in claim 40.

At column 15, lines 45-62, Kovacevic et al. discloses:

> At step 215, a determination is made whether the packet is a packet that is to be additionally parsed. For example, step 215 specifically indicates that a determination is being made whether the PID value indicates the packet is a video packet. If so, flow proceeds to step 226 for video parsing as indicated in FIG. 22. If the PID does not indicate a packet for special processing, i.e. not a video packet, the flow proceeds to step 227 where the data is send the buffer controller for storage, as indicated with reference to FIG. 22.

> When the PID allocation table, or other means, indicates the packet is a video packet the Packetized Elementary Stream Parser (PESP) is enabled to allow further processing. In the specific embodiment of the PID allocation table listed above, the video PID is stored as PID_0. However, other methods of identifying the video PID, such as the use of a flag or other indicator are also possible. The operation of the PESP is controlled by the PESP Control Registers, as illustrated in FIG. 18.

Contrary to the Examiner's allegation, nowhere in this section, or any other section, does Kovacevic et al. disclose or suggest a buffer configured to temporarily store data from a plurality of streams of variable speeds in a plurality of entries, as recited in claim 40. As explained above with regard to claim 1, Kovacevic et al. is silent with regard to steams of variable speeds.

Further, Kovacevic et al. does not disclose or suggest a counter that is configured to determine a number of entries in the buffer corresponding to each of the streams of variable speeds, as also recited in claim 40.

The Examiner did not specifically address this feature of claim 40. Therefore, the Examiner did not establish a proper case of anticipation with regard to claim 40.

When rejecting claim 16, however, the Examiner alleged that Kovacevic et al. discloses a counter that is configured to determine a number of entries in the buffer corresponding to each of the streams and cited column 15, lines 45-62, of Kovacevic et al. for support (Office Action, paragraph 17). Applicants respectfully disagree.

Column 15, lines 45-62, of Kovacevic et al. is reproduced above. Contrary to the Examiner's allegation, nowhere in this section, or any other section, does Kovacevic et al. disclose or remotely suggest a counter that is configured to determine a number of entries in the buffer corresponding to each of the streams of variable speeds, as required by claim 40.

Further, Kovacevic et al. does not disclose or suggest a comparator configured to determine whether to initiate flow control for each of the streams based on the determined number of entries for the stream, as also recited in claim 40.

The Examiner did not specifically address this feature of claim 40. Therefore, the Examiner did not establish a proper case of anticipation with regard to claim 40.

When rejecting claim 16, however, the Examiner alleged that Kovacevic et al. discloses a comparator configured to determine whether to initiate flow control for each of the streams based on the determined number of entries for the stream and cited column 15, lines 45-62, of Kovacevic et al. for support (Office Action, paragraph 17). Applicants respectfully disagree.

Column 15, lines 45-62, of Kovacevic et al. is reproduced above. Contrary to the Examiner's allegation, nowhere in this section, or any other section, does Kovacevic et al. disclose or remotely suggest a comparator configured to determine whether to initiate flow control for each of the streams of variable speeds based on the determined number of entries for the stream, as required by claim 40.

For at least these reasons, Applicants submit that claim 40 is not anticipated by Kovacevic et al. Claims 41-47 depend from claim 40 and are, therefore, not anticipated by Kovacevic et al. for at least the reasons given with regard to claim 40.

Independent claims 48 and 55 recite features similar to features recited in claim 40. Claims 48 and 55 are, therefore, not anticipated by Kovacevic et al. for at least reasons similar to reasons given with regard to claim 40. Claims 49-54 depend from claim 48 and are, therefore, not anticipated by Kovacevic et al. for at least the reasons given with regard to claim 48.

Independent claims 56 and 57 recite features similar to features recited in claim 1. Claims 56 and 57 are, therefore, not anticipated by Kovacevic et al. for at least reasons similar to reasons given with regard to claim 1.

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of the application and the timely allowance of pending claims 1-57.

If the Examiner does not believe that all pending claims are now in condition for allowance, the Examiner is urged to contact the undersigned to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

Paul A. Harrity
Reg. No. 39,574

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11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
(571) 432-0800